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PRODUCTS ENGINEERING MEASUREMENT

SILICON HETEROJUNCTION TRANSISTOR

Quarterly Report

prepared for the

U. S. Army Signal Supply Agency
225 South 18th Street
Philadelphia 3, Pennsylvania

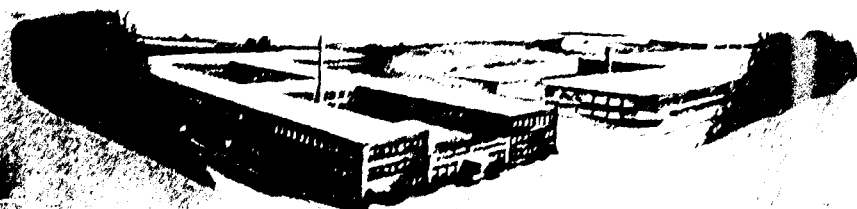
PERIOD COVERED

1 July 1961 to 30 September 1961

CONTRACT NO. DA-36-039-SC-81286

ORDER NO. 7633-PP-59-81-81

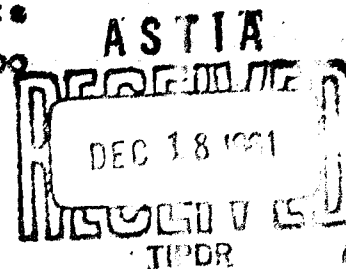
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Wakefield, Massachusetts

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PRODUCTION ENGINEERING MEASURE
ON
SILICON HIGH FREQUENCY POWER TRANSISTOR
QUARTERLY REPORT

OBJECTIVE: To develop, build and run a pilot line in the performance of a Production Engineering Measure on a Silicon High Frequency Power Transistor for operation at 10 Mc with 5 Watts output. The unit to be suitable for operation at 150 volts or lower over the temperature range from -65°C to 200°C with a 15 db power gain at 5 watts output at a minimum efficiency of 50 per cent.

CONTRACT NUMBER: DA-36-039-SC-81286

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SPECIFICATIONS: MIL-T-19500A

REQUIREMENT: Signal Corps Technical Requirement SCS-39

REPORT WRITTEN BY: David O'Brien

TABLE OF CONTENTS

	<u>Page</u>
LIST OF TABLES -----	1
LIST OF ILLUSTRATIONS -----	2
I PURPOSE -----	3
II ABSTRACT -----	4
III 5 WATT 10 Mc SILICON TRANSISTOR -----	5
A. The Base Diffusion -----	5
B. The Triple Diffused Transistors -----	8
C. The Emitter and Base Contacts -----	11
D. The Pilot Line -----	12
IV PROGRAM FOR NEXT QUARTER -----	13
V KEY TECHNICAL PERSONNEL -----	14
VI TIME EXPENDED DURING THIS QUARTER -----	14

LIST OF TABLES

1. Comparison of three methods of Phosphorus Back Diffusion. (Page 7)
2. $V_{ce_{sat}}$ and I_{co} of Triple Diffused Transistors. (Page 10)

LIST OF ILLUSTRATIONS

1. $V_{ce_{sat}}$ and V_{be} traces for triple and double diffused transistors. (Page 9)

I PURPOSE

The purpose of this Production Engineering Measure is to perform all the work necessary to establish the capability to manufacture the contract items on a pilot line basis using production methods and processes. The work shall include, but not be limited to the following specific tasks:

- A. Engineering necessary to establish production methods for the device.
- B. Design development, procurement of equipment and machinery to produce devices on a limited basis.
- C. The manufacture and submission of samples for approval and standardization.
- D. Production engineering to establish manufacturing techniques for the production of the approved standardized devices.
- E. Limited pilot production of the approved device and obtaining approval of the manufactured units.

II ABSTRACT

The work done during this quarter was directed at improving the $V_{ce_{sat}}$ of the 5 Watt 10 Mc Transistor. The results showed that a transistor with a N doped collector of 3 ohm bulk resistivity and 2 mils thick would have a $V_{ce_{sat}}$ less than the specified 1.7 volts, with $I_c = 500$ ma and $I_b = 200$ ma. The problems of making a transistor with a low $V_{ce_{sat}}$ were outlined in the last Quarterly Report. Some transistors have been produced with a low $V_{ce_{sat}}$ but the techniques involved in producing large numbers of these transistors with a high yield have not yet been mastered.

Work has been carried out on improving the emitter and base contacts with a resulting higher yield from these operations.

III 5 WATT 10 Mc SILICON TRANSISTOR

A. Back Diffusion

Experiments have been carried out on the back diffusion of P_2O_5 into silicon to provide a highly doped collector for the transistor. The transistors which were made from these back diffused slices showed that a transistor with a collector of 3 ohm material, 2 mils thick would have a $V_{ce_{sat}}$ of less than 1.7 volts.

The main problems arising from the back diffusion were :-

- a. Obtaining a deep phosphorus diffusion so that the slices would be a sufficient thickness to avoid serious loss in yield due to breakage.
- b. Controlling the surface preparation and thickness of the high resistivity part of the back diffused slice.

The diffusion of phosphorus into silicon is governed by the equation

$$C = C_0 \operatorname{erf} \frac{x}{2\sqrt{Dt}}$$

where C_0 = Surface concentration of phosphorus

C = Concentration of phosphorus at a distance x from the surface

D = Diffusion constant of phosphorus

t = Time.

It can be seen that to diffuse the phosphorus in a suitable depth the surface concentration must be maintained as high as possible.

The temperature during diffusion must be such that the silicon material is not damaged by the prolonged heat treatment, while ensuring that the phosphorus penetrates a distance suitable for transistors to be processed.

Three methods of phosphorus back diffusion are being tried, and are outlined below:

METHOD 1

The method tried first entailed depositing P_2O_5 on the slices in a double zone furnace under extremely dry conditions. For the deposition, the phosphorus source is at a temperature of $265^{\circ}C$, and the slice temperature is at $1250^{\circ}C$. After two hours, the slices are removed and placed in another furnace at $1250^{\circ}C$ and diffused for 200 hours. The depth of phosphorus in this diffusion is 3.5 mils. The junction obtained is parallel to the surface of the slice and the surface remains undamaged.

If instead of removing the slices from the phosphorus deposition furnace, we leave them in the same tube for a constant-source diffusion, the penetration of the phosphorus during the same time interval is increased to 4.0 mils. The junction obtained by this method has not been sufficiently deep to allow processing of transistors due to the large amount of breakage caused when operating with a slice of 6 mils thickness.

METHOD 2

Deeper penetrations of phosphorus have been obtained by painting a solution of P_2O_5 and water onto the silicon slices and then diffusing.

Penetrations of 5.5 mils have been obtained by this method when diffusing for 100 hours at 1350°C. When the slices are diffused for 200 hours at 1350°C, the penetration increases only 15% to 6.2 mils.

This method is unsatisfactory because of the inability to control the amount of phosphorus placed on the surface of each slice. Thus, slices in the same diffusion will have a different penetration of phosphorus. The penetration varies over the slice area and so the junctions obtained are not parallel to the surface.

METHOD 3

In this diffusion, the slices are placed together with the P_2O_5 in a vacuum capsule and diffused in the furnace. The P_2O_5 vapor in the capsule supplies a constant source as long as there is no moisture present. If there is moisture in the P_2O_5 , an oxide will form on the slices and so limit the P_2O_5 source. This method has given the deepest penetrations, but, like Method 2, it gives unreliable penetrations.

Table 1 compares the results of the 3 methods tried.

TABLE 1

Method	Depth In Mils				Parallelism of Junction
	1250°C 100 hrs	1350°C 100 hrs	1250°C 200 hrs	1350°C 200 hrs	
1	2.5	3.5	3.5	4.5	Good
2	3.0	5.5	4.5	6.2	Poor
3	4.3	6.2	5.1	7.1	Poor

B. Triple Diffused Transistors

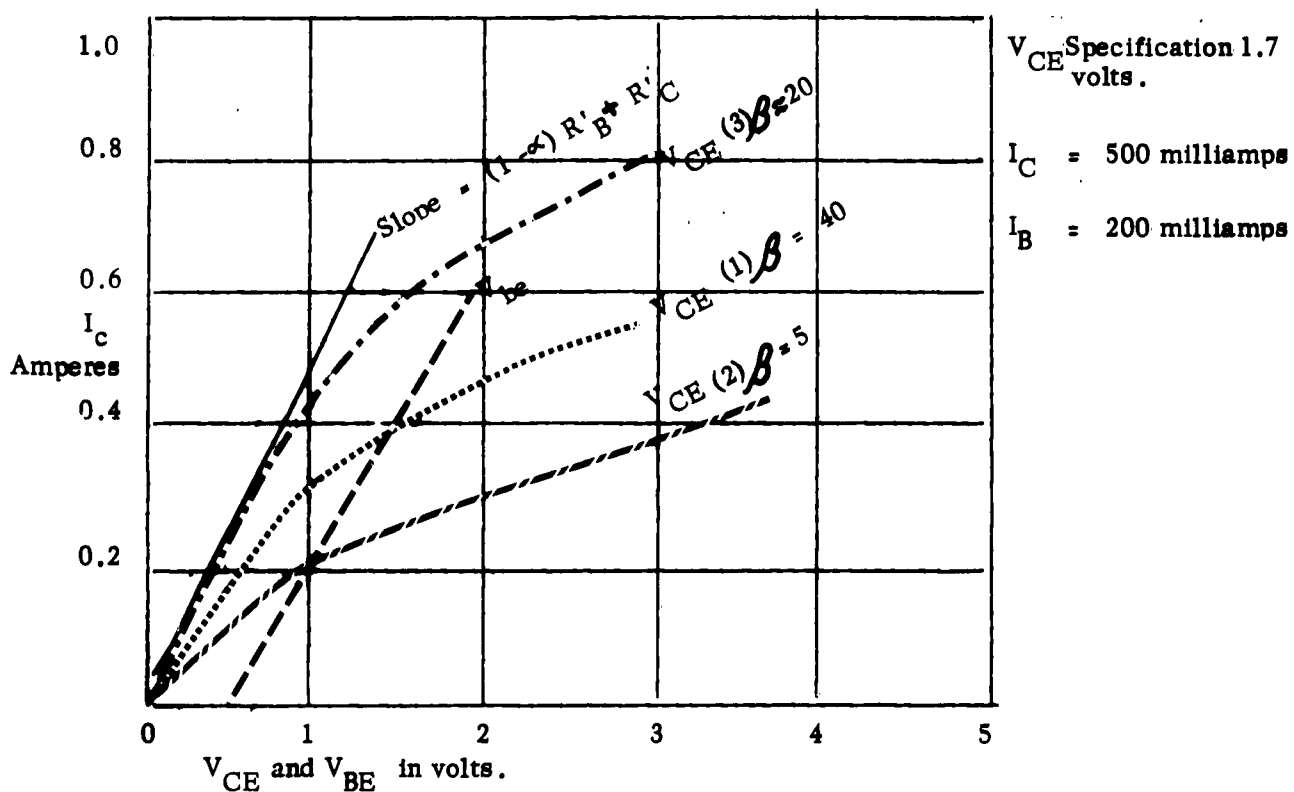
A small number of transistors have been made on back diffused slices. The collector contact which is gold doped with antimony is much improved over that on transistors made without back diffusion. The 2 mil high-resistivity region affords the 150 volt breakdown and gives a $V_{ce\text{ sat}}$ of less than 1 volt with $I_c = 500\text{ ma}$, $I_b = 200\text{ ma}$.

Figure 1 shows V_{ce} and V_{be} traces for typical transistors as shown in the last quarterly report. On the same diagram, there is now shown the same traces for the back diffused transistors which have been made. It will be noticed that the V_{ce} trace for the back diffused transistor follows the slope $(1-\alpha) R_b' + R_c'$ to a much higher value of I_c than the other transistors.

The $V_{ce\text{ sat}}$ of triple diffused transistors still depends on the beta of the transistors, but even low beta transistors have a $V_{ce\text{ sat}}$ less than 1.7 volts. The V_{be} trace of the triple diffused transistor is identical to that of the double diffused transistors.

FIGURE 1

V_{CE} and V_{BE} Traces of Triple Diffused Transistor



V_{CE} Trace (1) Double Diffused Transistor with $\beta = 40$

V_{CE} Trace (2) Double Diffused Transistor with $\beta = 5$

V_{CE} Trace (3) Triple Diffused Transistor with $\beta = 20$

In Table 2, the leakage at 60 volts and $V_{ce\ sat}$ for typical triple diffused transistors is shown. In all cases the $V_{ce\ sat}$ is less than the specified 1.7 volts at $I_c = 500\ ma$.

The average leakage on these transistors is considerably higher than double diffused transistors. This is due to the difficulty of controlling the thickness of the high resistivity material on the back diffused slices and at the same time preparing a surface suitable for the base-collector junction, i.e. free of dislocations and etch pits.

TABLE 2
 $V_{ce\ sat}$ and I_{co} of Triple Diffused Transistors

Transistor	$V_{ce\ sat}$ $I_c = 500\ ma$ $I_b = 200\ ma$ (volts)	I_{co} $V_{cb} = 60\ V$ (micro amps)
1	1.0	0.012
2	0.9	0.36
3	0.75	500.0
4	1.0	7.00
5	0.8	250
6	1.0	5.0
7	0.8	0.060
8	0.85	1.8
9	0.85	300.0
10	0.8	0.9

C. The Emitter and Base Contacts

Work has been done on the emitter and base contacts with a resulting higher yield from this operation.

The problem has been to put a thick layer of aluminum on the slice and then to remove the aluminum from all of the slice except where the contacts will be.

This has been done in the past by using mixtures of KMER and thinner and using sodium hydroxide to etch away the excess aluminum. The removal of the aluminum is very critical, as any aluminum left on the emitter base junction will cause an emitter base short.

The main source of trouble was the unreliability of the KMER operation. After developing the KMER, the slices usually had a cloudy film on them due to the KMER, and this slowed down the etching time of the aluminum. By using a KMER mixture without adding any thinner, the cloudy film can be removed by rubbing the slices with a cotton swab. This can only be done if straight KMER is used, because a rubbing operation will damage the photo-resist layer if the KMER is used with the thinner. However, the KMER usually needs thinner added to obtain good definition of the contacts. This problem was solved by developing the KMER with a fast jet of developer. The viscosity of the KMER is measured before use, and only that within a specified range is used.

Precautions are taken to prevent any dust settling on the KMER layer, because this impedes the removal of the KMER during the developing operation. Any KMER which is left on the emitter-base junction will protect the aluminum during the etching and so cause an emitter-base short.

D. The Pilot Line

A new location for the 5 watt 10 Mc transistor pilot line has been set up. This new location affords additional space and the efficiency of the line should improve. The facilities include a new dark room for the photo-resist. work, which has less variation in temperature and humidity.

Larger furnaces are being acquired capable of diffusing more slices at a time with better control over temperature. New masks have been designed to increase the number of potential transistors per slice and to reduce the size of the transistor die. The reduction in size of the die will reduce the loss of transistors due to cracking when being mounted on the header.

IV PROGRAM FOR NEXT QUARTER

Plans for the next quarter are to extend the work of the last quarter on back diffusion and also on the mechanical problems involved in producing a 2 mil high-resistivity region with a good surface. Investigations into electrochemically polishing high resistivity silicon material will be undertaken to achieve this end.

V. KEY TECHNICAL PERSONNEL

Navon, D.	Shapiro, G.
Rudenberg, G.H.	Lasch, K.
de Beurs, P	Dale, B.
O'Brien, D.	

VI TIME EXPENDED

<u>Month</u>	<u>Engineering Time</u>	<u>Technician Time</u>
July	364 hours	116 hours
August	400 hours	168 hours
September	<u>300 hours</u>	<u>104 hours</u>
<u>TOTALS</u>	<u>1,064 hours</u>	<u>388 hours</u>